Amendments to the Claims:

Please amend claims 1, 5, 7 and 9 and add claims 10-13 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A vertical trench-gate semiconductor device comprising:

a semiconductor body having a top major surface, and

a plurality of trench-gates comprising trenches extending into the semiconductor body from the top major surface with insulated gate electrodes therein,

the semiconductor body comprising source and drain regions of a first conductivity type that are separated by a channel-accommodating region of a second, opposite conductivity type adjacent the trench-gates, wherein

the trench-gates extend in stripes,

the source regions extend transversely between the trench-gates in stripes, projection of the source stripes across the trench-gates defines intermediate trench portions between the projected source stripes, and mutually spaced regions of the second conductivity type are provided immediately below the intermediate trench portions that are connected to source potential, wherein each of said spaced regions extends from the channel-accommodating region on one side of a trench to meet the channel-accommodating region on the other side of the trench, wherein the spaced regions are narrower than the intermediate trench portions.

2. (previously presented) The vertical trench-gate semiconductor device as recited in claim 1, wherein each of said spaced regions is an extension of the channel-accommodating region.

3. (canceled)

4. (previously presented) The vertical trench-gate semiconductor device as recited in claim 1, wherein the depth of each trench oscillates along its length between depths above and below the lower boundary of the channel-accommodating region, such that the second conductivity type region that provides the channel-accommodating region extends periodically below the trench to form the space regions.

5. (currently amended) A method of manufacturing a vertical trench-gate transistor semiconductor device comprising the steps of:

(a) forming a first mask over a top major surface of a semiconductor body defining a striped pattern of windows;

(b) introducing dopant of a first conductivity type for a source region into the semiconductor body via the windows of the first mask;

(c) forming a second mask over the top major surface of the semiconductor body defining a striped pattern of windows that extend transversely to the striped windows of the first mask;

(d) introducing an etchant via the windows of the second mask to form trenches in the semiconductor body, the etchant being selected to etch both the semiconductor body and the first mask material, such that the resulting trenches are deeper than the lower boundary of a channel-accommodating region in the finished device within the lateral extent (L) of the first mask windows and shallower than said lower boundary between the first mask windows to form mutually spaced regions of a second conductivity type, wherein each of said spaced regions extends from the channel-accommodating region on one side of a trench to meet the channel-accommodating region on the other side of the trench, wherein the spaced regions of the second conductivity type are provided immediately below intermediate trench portions, and wherein the spaced regions are narrower than the intermediate trench portions.

6. (previously presented) The method of claim 5, wherein the etchant etches the first mask material more slowly than the semiconductor body.

7. (currently amended) A method of manufacturing a vertical trench-gate transistor semiconductor device comprising the steps of:

etching grooves of uniform depth into a semiconductor body, and

selectively etching portions of the grooves, such that the resulting trenches are deeper than the lower boundary of a channel-accommodating region in the finished device within the lateral extent (L) of source region stripes and shallower than said lower boundary between the source region stripes to form mutually spaced regions of a conductivity type, wherein each of said spaced regions extends from the channel-accommodating region on one side of a trench to meet the channel-accommodating region on the other side of the trench, wherein projection of the source region stripes across the trench-gates defines intermediate trench portions between the projected source region stripes, and wherein the spaced regions are narrower than the intermediate trench portions.

8. (previously presented) A method of manufacturing a vertical trench-gate transistor semiconductor device of claim 1 having trenches of substantially uniform depth, comprising the steps of:

forming a mask over the top surface of the semiconductor body; and

introducing dopant of the second conductivity type through the windows of the mask for the spaced regions.

9. (currently amended) The vertical trench-gate semiconductor device as recited in claim 1, wherein each of said spaced regions does not extend into the drain ~~regions~~ region of the semiconductor body.

10. (new) The vertical trench-gate semiconductor device as recited in claim 1, wherein the drain region include a drain drift region, and wherein each of the spaced regions extends downwardly into the drain drift region from the channel-accommodating region adjacent to one side of the trench, along the sidewall of the trench, adjacent to the bottom of the trench and then up the other sidewall of the trench to rejoin the channel-accommodating region on the other side of the trench.

11. (new) The vertical trench-gate semiconductor device as recited in claim 1, wherein each of the spaced regions only contacts the channel-accommodating region on one side of the trench to provide a connection to the source potential.

12. (new) The vertical trench-gate semiconductor device as recited in claim 1, wherein a thickness of the spaced regions is minimized and the spaced regions are as low doped as possible without causing the spaced regions to be depleted completely during a normal use of the vertical trench-gate semiconductor device.

13. (new) The vertical trench-gate semiconductor device as recited in claim 12, wherein the thickness of the spaced regions is in the vertical direction and perpendicular to the top major surface.